



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,250	09/17/2003	Luc Minnebo	GN03078	1130
21013	7590	07/05/2007	EXAMINER	
AGFA CORPORATION PATENT DEPARTMENT 200 BALLARDVALE STREET WILMINGTON, MA 01887			BURLESON, MICHAEL L	
		ART UNIT	PAPER NUMBER	
		2625		
		MAIL DATE	DELIVERY MODE	
		07/05/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,250	MINNEBO, LUC	
	Examiner	Art Unit	
	Michael Burleson	2625	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-11 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-11 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over U.S. Patent No. 6637851 in view of U.S Publication 2004/0113958.

3. Regarding claim 1, claim 1 of US patent 6637851 teaches a method for reproducing on an output device an electronic image having colour pixels, each colour

pixel being represented by K spatially corresponding component pixels, $K \geq 1$, each component pixel having an input pixel value, the output device being capable of rendering $N_{sub,j}$ intensity levels for a component pixel j, $1 \leq j \leq K$, thereby defining $N_{sub,1} * N_{sub,2} * \dots * N_{sub,K}$ intensity level combinations, the method comprising the steps of: computing for any colour pixel a scalar value which is a function of at least one of said input pixel values of said spatially corresponding component pixels; quantizing said scalar value by a multilevel halftoning process to obtain for said colour pixel a quantized scalar value; using said quantized scalar value to select, out of all said intensity level combinations, a subset of intensity level combinations; selecting one combination out of said subset; using said selected combination for reproducing said colour pixel by said output device.

US patent 6637851 fails to teach of method for creating at least one printing master comprising the steps of: providing a printing master precursor, selectively creating ink-carrying and non ink-carrying areas on said printing master precursor by means of an ink jet printing system printing dots on the printing master precursor wherein the position of the dots is controlled with an increment that is less than the size of the smallest dot, characterized in that the position of the dots is controlled by a sub-dot phase modulation error diffusion algorithm.

Claim 1 of U.S Publication 2004/0113958 teaches of method for creating at least one printing master comprising the steps of: providing a printing master precursor, selectively creating ink-carrying and non ink-carrying areas on said printing master

precursor by means of an ink jet printing system printing dots on the printing master precursor wherein the position of the dots is controlled with an increment that is less than the size of the smallest dot, characterized in that the position of the dots is controlled by a sub-dot phase modulation error diffusion algorithm.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify US patent 6637851 wherein US patent 6637851 device is applied to computer to plate printing. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify US patent 6637851 by the teaching of U.S Publication 2004/0113958 in order to make printing masters, page 1,paragraph 0003.

4. Regarding claim 2, claim 2 of the present invention corresponds to claim 2 of U.S Publication 2004/0113958.

5. Regarding claim 3, claim 3 of the present invention corresponds to claim 2 of U.S patent 6637851.

6. Regarding claim 4, claim 4 of the present invention corresponds to claim 3 of U.S patent 6637851.

7. Regarding claim 6, claim 6 of the present invention corresponds to claim 7 of U.S Publication 2004/0113958.

8. Regarding claim 8, claim 8 of the present invention corresponds to claim 5 of U.S Publication 2004/0113958.

9. Regarding claim 9, claim 9 of the present invention corresponds to claim 6 of U.S Publication 2004/0113958.

10. Regarding claim 10, claim 10 of the present invention corresponds to claim 9 of U.S Publication 2004/0113958.

11. Regarding claim 11, claim 1 of US patent 6637851 teaches a method for reproducing on an output device an electronic image having colour pixels, each colour pixel being represented by K spatially corresponding component pixels, $K > 1$, each component pixel having an input pixel value, the output device being capable of rendering $N_{sub,j}$ intensity levels for a component pixel j, $1 \leq j \leq K$, thereby defining $N_{sub,1} * N_{sub,2} * \dots * N_{sub,K}$ intensity level combinations, the method comprising the steps of: computing for any colour pixel a scalar value which is a function of at least one of said input pixel values of said spatially corresponding component pixels; quantizing said scalar value by a multilevel halftoning process to obtain for said colour pixel a quantized scalar value; using said quantized scalar value to select, out of all said intensity level combinations, a subset of intensity level combinations; selecting one combination out of said subset; using said selected combination for reproducing said colour pixel by said output device.

US patent 6637851 fails to teach of method for creating at least one printing master comprising the steps of: providing a printing master precursor, selectively creating ink-carrying and non ink-carrying areas on said printing master precursor by means of an ink jet printing system printing dots on the printing master precursor wherein the position of the dots is controlled with an increment that is less than the size of the smallest dot, characterized in that the position of the dots is controlled by a sub-dot phase modulation error diffusion algorithm.

Claim 1 of U.S Publication 2004/0113958 teaches of method for creating at least one printing master comprising the steps of: providing a printing master precursor, selectively creating ink-carrying and non ink-carrying areas on said printing master precursor by means of an ink jet printing system printing dots on the printing master precursor wherein the position of the dots is controlled with an increment that is less than the size of the smallest dot, characterized in that the position of the dots is controlled by a sub-dot phase modulation error diffusion algorithm.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify US patent 6637851 wherein US patent 6637851 device is applied to computer to plate printing. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify US patent 6637851 by the teaching of U.S Publication 2004/0113958 in order to make printing masters, page 1,paragraph 0003.

Claims 5 and 7 are rejected for depending on claim 1.

Allowable Subject Matter

12. Claims 1-11 would be allowable if the Double Patenting rejection is overcome.

Conclusion

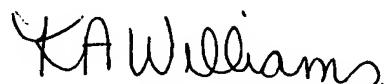
1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Burleson whose telephone number is 571-272-

Art Unit: 2625

7460. The examiner can normally be reached Monday through Friday from 8:30 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler Lamb can be reached on 571-272-7406.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael Burleson

Patent Examiner

KIMBERLY WILLIAMS
PRIMARY PATENT EXAMINER



June 24, 2007